The reason it is also known as the counter type ADC is because it uses the binary counter for the conversion.

As the counter increment its count, the output of the DAC increment in ramp fashion.

If you see the DAC output, it looks like a staircase.

The output of the counter is given to the input to the DAC.

Initially, when the conversion starts, the counter is resent. That is why the output of DAC is equal to 0.

So initially, >

That is why the output of the comparator is high.

The clock pulses are applied to the counter using AND gate.

So whenever the output of the comparator is high, at this time these clock pulses will be applied to the counter.

And due to that, the counter starts counting.

As the counter increments its count, the output of the DAC will also increase in the staircase fashion.

The output of the DAC is countinously compared with the input voltage.

So as far as the , < , the output of the comparator will be high.

And due to that these clock pulses will be applied to the counter.

Hence the output of the DAC will gradually increase in staircase fashion.

As soon as > , then the output of the comparator will be low.

And now, no clock pulses will be applied to the counter.

This counter will be reset.

Once again the new convrsion will start.

This means the new input value will get sampled and the new conversion will start.

Every time the new conversion starts, the counter will be reset.

This means every time the counter starts from 0 onwards.

We can say that the conversion time depends on the magnitude of the input voltage.

The larger the input voltage, the more time ADC will take for the conversion.

